Competitive Exams: Design of CPU

The CPU can be designed from the hardware specifications and by loading-the binary micro program into control memory. The memory unit stores the instructions, data, and other binary coded information needed by the processor. It is assumed that the access time of the memory is fast enough for the CPU to be able to read, or write a word within one clock pulse period. Even though this restriction is not always applicable in a computer system, we assume it here in order to avoid complicating the design with a wait period that stops the operations within the CPU until the memory cycle is completed.

The interface units provide a path for transferring information between the CPU and external input or output devices connected through the I/O bus. We assume a memory-mapped I/O method of addressing between the CPU and the registers in the interface units. By this method, there are no input or output instructions in the computer because the CPU can manipulate the data residing in interface registers with the same instructions that are used to manipulate memory locations. Each interface unit is organized as a set of registers that respond to the read or write signals in the normal! address space of the 16-bit address. Typically, the bulk of the address space is assigned to memory words and a small segment is reserved for interface registers.

The communication between the CPU and external modules takes place via the address and the data buses. The address bus consists of 16 lines and is unidirectional horn the CPU to the other units. The data bus also consist of 16 lines but is bidirectional, allowing the information to flow in either direction. The read and write control lines from the CPU specify the direction to transfer in the data bus. The read signal informs the selected memory word or interface register to transfer data into the CPU. The write signal informs the selected unit that a data word is available for transfer from the CPU to the selected memory word or interface register.

1. Arithmetic Logic Shift Unit (ALSU) : The arithmetic logic shift unit (ALSU) is a combinational circuit that performs a-number of arithmetic, logic, and shift micro operations. The control unit activates the micro operations when it executes the instructions jn the program. The ALSU has a number of selection lines to select a particular operation in the unit. The selection variables are decoded by means of multiplexers so that k selection variables can specify up to two distinct operations.

2. Processor Unit: It consists of a file of 14 registers, an ALSU, and three buses that provide the data path within the unit. Two sets of multiplexers select a register or the input data for the ALSU. A decoder selects a destination register by enabling its load input. All registers and the input and output data are 16 bits of the control word that select a micro-operation in the processor unit ire divided into four fields: The A field specifies the input to the left side of the ALSU. The B field specifies the input to the right side of the ALSU. The D field specifies the destination register. The 14 registers in the processor unit are assigned special tasks by the CPU. The first eight registers, designated RO through R7, are available to the user as general purpose registers that can he manipulated by program instructions. One register acts as a program counter and the other five registers are used by the control unit for storing temporary results. The status bits associated with the ALSU are symbolized. They are altered to reflect
3. the result of the carry, zero, sign and overflow in the ALSU.

Programmer Model

Eight processor registers are used for manipulating data through program instructions. The last two registers are used as stack pointer and index register. The program counter can be changed by the programmer by means of branch type instructions. The status bits are affected by certain ALSU operations. The other parts of the computer of interest to the user are the ALSU, the memory unit, and the input and output addresses of external devices.

Even though the user and programmer can communicate with only 9 registers, there are actually 20 registers in the CPU. The other 11 registers are exclusively used by the control unit for internal operations.